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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,553	05/18/2005	William Donaldson	US02 0454 US	7482
24738 7590 01/19/2007 PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131			EXAMINER TRA, ANH QUAN	
			ART UNIT	PAPER NUMBER
			2816	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		01/19/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/535,553

Applicant(s)

DONALDSON ET AL.

Examiner

Quan Tra

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to the amendment filed 11/29/06. The rejections in previous office action are maintained.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6-12, 14-16, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Buhring (EP 1065600), Applicant's submitted IDS.

As to claim 1, Buhring's figure shows a device comprising: a floating bus (CHN_H, CHN_L); power and data system (6-8, 11, 18, 19) for driving the floating bus, the power and data system comprising a charge pump circuit; and at least one switch control circuit (9, 10, 14, 15, 20) coupled to the floating bus and the power and data system for facilitating charging of the floating bus and for controlling electromagnetic emission from the device (it is inherent that circuit (9, 10, 14, 15, 20) controls some of or little the EME of the circuit).

As to claim 2, the figure shows that the at least one switch control circuit comprises a first switch control circuit and a second switch control circuit, the first switch control circuit comprising at least one P type transistor circuit (9), and the second switch control circuit comprising at least one N type transistor circuit (10) and wherein the first switch control circuit and the second switch control circuit comprise complementary circuits.

As to claim 3, the figure shows that the first switch control circuit is electrically connected to a first bus node of the floating bus and the second switch control circuit is electrically connected to a second bus node of the floating bus.

As to claim 4, the figure shows that the charge pump circuit comprises an integrated circuit employing at least one transistor and diode pair.

As to claim 6, the figure shows that the floating bus comprises a balanced bus system having a high side bus node and a low side bus node, and wherein the at least one switch control circuit comprises a first switch control circuit and a first diode connected to the high side bus node and a second switch control circuit and a second diode connected to the low side bus node.

As to claim 7, the figure shows that the first switch control circuit and the second switch control circuit are driven by a reference circuit (circuit, not shown, that providing supply voltages to circuit 14 and 15), the reference circuit generating a first reference signal for the first switch control circuit and a second reference signal for the second switch control circuit.

As to claim 8, the figure shows that when a voltage across a first terminal and a second terminal of the first switch control circuit is greater than a threshold value (a threshold value may be any value), output current from the first switch control circuit is constant at a value dependent on the first reference signal (clearly the output current is dependent on the power supply voltage of 14 and 15), and when voltage across a first terminal and a second terminal of the second switch control circuit is greater than the threshold value, output from the second switch control circuit is constant at a value dependent on the second reference signal.

As to claim 9, the figure shows that the at least one switch control circuit controls electromagnetic emission from the device by constraining the slew rate on the floating bus.

As to claim 10, the figure shows a circuit comprising: a first switch control circuit (9, 20, 14) for electrical coupling to a high side bus node of a floating bus, and a second switch control circuit (10, 15) for electrical coupling to a low side bus node of the floating bus, wherein the first switch control circuit and the second control circuit comprise complementary circuits for

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controlling charging of the floating bus by a power and data system; and a reference circuit for generating a first reference signal for the first switch control circuit and a second reference signal for the second switch control circuit, wherein the first reference signal and the second reference signal are employed by the first switch control circuit and the second switch control circuit, respectively, for controlling electromagnetic emissions from the floating bus by constraining a slew rate on the floating bus.

As to claim 11, the figure shows that the power and data system comprises a charge pump circuit, the charge pump circuit comprising an integrated circuit.

As to claim 12, the figure shows that the first switch control circuit comprises a P type transistor circuit, and the second switch control circuit comprises a complementary N type transistor circuit.

As to claim 14, the figure shows a method comprising: tailoring a transfer characteristic of a first switch control circuit (9, 14, 20) to be electrically coupled to a high side bus node of a floating bus, and tailoring a transfer characteristic of a second switch control circuit (10, 15) to be electrically coupled to a low side bus node of the floating bus, wherein the first switch control circuit and the second switch control circuit comprise complementary control circuits for controlling charging of the floating bus by a power and data system; and generating, when in use, a first reference signal (power supply of 14) for the first switch control circuit and a second reference signal (power supply of 15) for the second switch control circuit, wherein the first reference signal and the second reference signal are employed by the first switch control circuit and the second switch control circuit, respectively, for controlling electromagnetic emission from the floating bus by constraining a slew rate on the floating bus.

As to claim 15, the figure shows that the power and data system comprises a charge pump circuit, the charge pump circuit comprising an integrated circuit.

As to claim 16, the figure shows the step of integrating the first switch control circuit and the second switch control circuit on the integrated circuit with the charge pump circuit.

Claim 18 recites similar limitations of claim 10. Therefore, it is rejected for the same reasons.

As to claim 19, the figure shows that the switch control circuit includes: a switch (9) selectively connecting the floating bus to the power and data system; and slew rate adjusting means (20) for adjusting a slew rate of a voltage on the floating bus when the switch connects floating bus to the power and data system.

As to claim 20, the figure shows that the slew rate adjusting means is responsive to a reference current (current generated by 15), wherein when the reference current has a first value (when 20 is off), the slew rate adjusting means adjusts the slew rate of the floating bus to be a first slew rate, and wherein when the reference current has a second value (when 20 is ON), the slew rate adjusting means adjusts the slew rate of the floating bus to be a second slew rate greater than the first slew rate.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 5, 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buhning (EP 1065600) in view of Yamanaka (US 20020154524).

Buhning's figure shows all limitations of the claims except for that "the at least one switch control circuit is operable in at least a low speed mode and a high speed mode, with mode of the at least one switch control circuit being dependent upon a desired floating bus charging

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speed". However, Yamanaka's figures 2-5 shows charge pump circuit having voltage detecting circuit (i.e. 2-11 and 22 in figure 2) for controlling the speed of the switches in order to reducing rush current. Therefore, it would have been obvious to one having ordinary skill in the art to employ Yamanaka teaching to control the switches' speeches of Buhring in order to reduce rush current.

Response to Arguments

5. Applicant's arguments have been fully considered but they are not persuasive.

Applicant argues that Buhring fails to teach "controlling electromagnetic emission from the device". The examiner respectfully disagrees. It is inherent that each of Buhring's circuit elements generates either none or some electromagnetic emissions respect to electrode magnetic field goes through the elements. The circuit comprising elements 9, 10, 14, 15 and 20 also generates either none or some electromagnetic emissions respect to the electromagnetic field. Thus, the generating of none or some electromagnetic emissions is considered as the claimed "controlling electromagnetic emission".

Applicant further argues that power supply voltage is not a signal. The examiner respectfully disagrees. With broadest reasonable interpretation, power supply voltage is a constant signal.

Applicant further argues that switches 9, 10 and 12 do not depend on any power supply. The examiner respectfully disagrees. The voltage levels of signals generated by circuits 14 and 15 turn ON/OFF and determine the current going through OFF switches 9, 10 and 12 (current of transistor is determined by gate-source voltage). Further, the output voltage levels of 14 and 15 are determined by the supply voltages of circuits 14 and 15. Therefore, currents through switches 9, 10 and 12 depend on the power supplies of circuit 14 and 15.

In response to the argument of the rejection of claim 9, slew rate is determined by the output current. Higher output current provides faster speed. The output current of only one ON transistor of circuit 9 and 20 is less than the output current of both ON transistors of circuit 9 and 20. Thus, circuit 9 and 20 controls the slew rate on the floating bus dependent on how many transistors are ON.

Applicant argues with the same reasons for the rejection of claims 10-12, 14-16 and 18. Therefore, similar responses are applied.

In response to the argument of the rejection of claim 5, Buhring fails to teach changing the speed of the switches. However, Yamanaka shows a similar circuit that is capable of changing the speed of the switches. Therefore, one skilled in the art would have motivated to employ Yamanaka's teaching in order to take advantage of Yamanaka's benefits, such as reducing rush current.

Applicant further argues that Office Action does not cite anything in Yamanaka that Teaches that any modes are dependent upon desired floating bus charging speed. The examiner respectfully disagrees. The circuit connection, the sizes of the elements, what output level that the switches will change speed are selected by one skilled in the art. Thus, the Yamanaka and the modified Buhring disclose that the modes are dependent upon a desired (selected by one skilled in the art) floating bus charging speed.

In response to the argument of the rejection of claims 13 and 17, as stated above, without power supplies, there is not control signal and control voltage. Therefore, the speed mode is determined by the power supply signals.

Prior art

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Eichfeld et al, USP 6531886 teaches capacitor reduces EMC. Buhning also shows capacitor coupled to the outputs. Buhning' capacitor is also considered as part of the switch control circuit.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Quan Tra', with a long horizontal flourish extending to the right.

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

January 11, 2007